What is claimed is:

1. A non-volatile semiconductor memory device comprising:

a cell array having electrically rewritable and non-volatile memory cells arranged to constitute at least one block with a plurality of pages; and

a controller for controlling data erase by a page or sub-block with plural and continuous pages in the block, wherein

said cell array has an erase control area set therein in which the number of data erase is stored as being expressed by a series of two-value data, the number of "0" data at lower bit side thereof indicating an accumulated value of the number of data erase in a block, and wherein

the number of data erase is read out before data erase for a selected page in said block by a check-read operation in which plural pages are simultaneously set at a selected state, and renewed and written into said selected page after data erase.

2. The non-volatile semiconductor memory device according to claim 1, wherein

said cell array has a normal data area, in which normal data read and write are performed, and a redundant area in which said erase control area is set.

3. The non-volatile semiconductor memory device according to claim 1, further comprising:

a sense amplifier circuit for data reading and writing by a page of said cell array;

a register circuit for temporarily holding the number of data erase read in said sense amplifier circuit from said erase control area before data erase;

a data transfer circuit configured to transfer the number of data erase read in said sense amplifier circuit to said register circuit, and add one to the number of data erase held in said register circuit to renew and transfer it to said sense amplifier circuit; and

a judgment circuit for judging whether the number of data

erase transferred to said register circuit reached to a permissible maximum value or not.

4. The non-volatile semiconductor memory device according to claim 3, wherein

said data transfer circuit comprises:

read-transfer buffers activated by a first timing signal to transfer the number of data erase read in said sense amplifier circuit to said register circuit in a bit-parallel state; and

write-transfer buffers activated by a second timing signal to shift the number of data erase toward upper bit side one by one, and add "0" data serving as the lowermost bit of the number of data erase to renew and transfer the number of data erase to said sense amplifier circuit.

5. The non-volatile semiconductor memory device according to claim 3, wherein

said judgment circuit is a comparator activated by a third timing signal to determine whether the uppermost bit of the number of data erase is logic "0" or "1".

6. The non-volatile semiconductor memory device according to claim 3, wherein

an output signal of said judgment circuit is output to external of the chip as a status flag.

7. The non-volatile semiconductor memory device according to claim 1, wherein

said cell array has NAND cell units arranged therein, each NAND cell unit being formed of plural memory cells connected in series with the respective control gates being connected to different word lines, a group of memory cells connected to a word line serving as one or two pages, a group of NAND cell units arranged in the direction of the word lines serving as a block.

8. An electric card equipped with a non-volatile semiconductor memory device defined in claim 1.

9. An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card defined in claim 8 and electrically connectable to said card slot.

10. The electric device according to claim 9, wherein said electric device is a digital still camera.

11. A non-volatile semiconductor memory device comprising:

a cell array having NAND cell units arranged therein, each NAND cell unit being formed of rewritable and non-volatile memory cells connected in series with the respective control gates being connected to different word lines, a group of memory cells connected to a word line serving as one or two pages, a group of NAND cell units arranged in the direction of the word lines serving as a block, said cell array being divided into a normal data area and a redundant area in the direction of the word lines, the number of data erase accumulated in a block being written into a page last selected for data erase in the block;

a sense amplifier circuit for data reading and writing by a page of said cell array, said sense amplifier having a normal sense amplifier circuit and a redundant sense amplifier circuit disposed corresponding to said normal data area and redundant area, respectively;

a controller for controlling data erase by a page or sub-block with plural and continuous pages in the block;

a register circuit for temporarily holding the number of data erase read in said redundant sense amplifier circuit from said redundant area before data erase;

a data transfer circuit configured to transfer the number of data erase read in said redundant sense amplifier circuit to said register circuit, and add one to the number of data erase held in said register circuit to renew and transfer it to said redundant sense amplifier circuit; and

a judgment circuit for judging whether the number of data erase transferred to said register circuit reached to a permissible maximum value or not.

12. The non-volatile semiconductor memory device according to claim 11, wherein

the number of data erase stored in said redundant area is expressed by a series of two-value data, the number of "0" data at lower bit side thereof indicating an accumulated value of the number of data erase in a block, and wherein

the number of data erase stored in said redundant area is read out to said redundant sense amplifier circuit before data erase for a selected page in said block, by a check-read operation in which plural pages are set at a selected state, and renewed and written back into said redundant sense amplifier circuit after data erase, and then written into said redundant area in said selected page.

13. The non-volatile semiconductor memory device according to claim 11, wherein

said data transfer circuit comprises:

read-transfer buffers activated by a first timing signal to transfer the number of data erase read in said redundant sense amplifier circuit to said register circuit in a bit-parallel state; and

write-transfer buffers activated by a second timing signal to shift the number of data erase toward upper bit side one by one, and add "0" data serving as the lowermost bit of the number of data erase to renew and transfer the number of data erase to said redundant sense amplifier circuit.

14. The non-volatile semiconductor memory device according to claim 11, wherein

said judgment circuit is a comparator activated by a third timing signal to judging whether the uppermost bit of the number of data erase is logic "0" or "1", an output signal thereof being output to external of the chip as a status flag.

15. An electric card equipped with a non-volatile semiconductor memory device defined in claim 11.

16. An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card defined in claim 15 and electrically connectable to said card slot.

17. The electric device according to claim 16, wherein said electric device is a digital still camera.